IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Confirmation No.: 8226

Kouichi IKEDA et al Art Unit: 2823

S. N. 09/716,843 Examiner: B. Kebede

Filed: November 17, 2000

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

BRIEF ON BEHALF OF APPELLANT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Examiner's final rejection mailed June 27, 2003.

REAL PARTY IN INTEREST

The real party in interest is Niigata Seimitsu Co., Ltd., the assignee of the application.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to appellant, the appellant's legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 5, 6, 8 and 9 are pending in the application, are rejected, and are the claims under appeal. Appellant wishes to prosecute this appeal with respect to claims 5, 6, 8 and 9. An appendix of claims is included herewith.

This application was originally filed on November 17, 2000, with claims 1-10. A restriction requirement was made and claims 1-4 were withdrawn. A first office action was mailed October 4, 2002, and a response to that action was filed April 4, 2003, amending claims 5 and 8 and canceling non-elected claims 1-4 and claims 7 and 10. A final office action was mailed July 30, 2003, and a notice of appeal was filed November 26, 2003, to which this present appeal brief relates. No amendments were made after final.

STATUS OF AMENDMENTS

No amendment was filed subsequent to final rejection.

SUMMARY OF THE INVENTION

The invention relates to a method for manufacturing semiconductor devices, ensuring maximum usage of semiconductor chip portions on a wafer. In making certain semiconductor devices, such as memory modules using memory chips, multichip modules are made to provide high density mounting. However, a single defective chip can render a module nonfunctional, and require it to be discarded. This results in low yield and low

efficiency (background art portion of specification, page 1, line 14 - page 2, line 10).

In the inventive method, a wafer 2 (FIG. 1B) has plural memory chips 1 formed thereon, dotted lines in FIG. 1B denoting individual memory chips. To make a memory module, these chips would be divided into groups of 4, 2 or 1 (FIG. 1C) (page 4, lines 18-24).

The chips are quality tested (page 5, line 11-15) on the wafer as a whole, and this can result in a map (FIG. 3A) of good chips (those that passed the quality test) and bad chips. In FIG. 3A, good chips are marked with an "O", while bad chips are marked with an "X". (page 3, line 20-26). From here, as shown in FIG. 3B, the chips may be divided into groups of passed chips for use in memory modules (in the case, given here as an example, where the semiconductor chips are memory chips). In FIG. 3B, the solid dark lines indicate borders for dividing the chips. (page 5, line 26-page 6 line 16). It is preferred, to give higher value or efficiency, to group the chips in the largest number of pieces as possible, 4 being the maximum in the illustrated embodiments. But, in accordance with the method, smaller group units of chips that passed the quality test are also available and used, reducing waste and increasing yield.

ISSUES

The broad issue presented in this appeal is whether the Examiner's final rejection of claims 5, 6, 8 and 9 is proper. The issue may be stated more narrowly as:

1. Whether claims 5, 6, 8 and 9 are indefinite under 35 U.S.C. §112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Whether claims 5, 6, 8 and 9 are unpatentable under 35 U.S.C. §102(e) as being anticipated by Cockerill et al (U.S. 5,786,237).

GROUPING OF CLAIMS

Claims 5, 6, 8 and 9 stand or fall together for the purposes of this appeal.

ARGUMENT

1. Claims 5, 6, 8 and 9 are definite. The Examiner rejected claims under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. The Examiner alleges that it is unclear, that the claims lack clarity in meaning and scope, taking the position that since the applicant "use an "if" statement the result "then" is missing as result of execution the task." (final office action page 2, numbered section 3, 3rd paragraph).

Applicant respectfully traverses. The claims are clear and conform to perfectly acceptable English language construction.

If we are to accept the Examiner's position, then it would be unclear for a person to say (or write) "I will come visit you if it is not snowing." Certainly some computer languages requires strict adherence to an "IF-THEN-ELSE" configuration, but English does not require this, nor does claim language construction. Applicant's position is that the language is perfectly clear as written. Even IF it was not clear, the specification, including the text and drawings, explain what is meant by this.

The Examiner seems to say that because applicant's claim does not have an explicit "IF-THEN" wording, that it is unclear. Such a conclusion is respectfully believed to be unreasonable. How can it be unclear to say (looking at claim 5 as an example) "dividing one of a plurality of pieces of said semiconductor chips on the basis of a result of said quality test, wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but . . . ". The claim goes on to add that they are divided into groups of two if groups of four are determined to be not possible, and to divide into groups of one if neither groups of four or groups or 2 are possible.

Applicant does not understand why the Examiner considers this to be unclear. It seems perfectly clear to us. The specification sets out what is happening, the language of the

claim is in acceptable English form, it is respectfully submitted that the claim is definite.

The Examiner further questions the limitation "to be possible", saying it is not certain "whether the determination is made to choose the selection of division of chips".

Again, applicant respectfully traverses the rejection. It is submitted that this is perfectly clear. The claim explicitly says that the dividing is made into "first groups of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test". This is respectfully believed to be clear and definite.

This clearly sets out that "the determination is made to choose the selection of division of chips".

The claim says that a step of dividing is done on the basis of a result of a quality test (that was performed in a previous step) and then the wherein clause of the claim further defines how that dividing takes place and it seems quite clear to applicant. Again, even if it was not clear on simply reading the claim (applicant believes it is clear, but is mentioning this for sake of argument), the specification discusses and shows what is meant, so it would be easy for the reader to understand what is meant by the claim and to interpret the claim. The claims are to be interpreted in light of the specification, so while the claims

are clear and definite on their face, even if they were not, the specification provides ample support to understand what is meant.

Claim 8 employs similar language and the Examiner makes the same rejection to claim 8 as to claim 5, so the above arguments are also applicable to claim 8. Claims 6 and 9 depend from the two independent claims, respectively.

It is submitted that claims 5, 6, 8 and 9 are in compliance with 35 U.S.C. §112, second paragraph, and it is requested that the Examiner's rejection under that statute be overruled.

2. Claims 5, 6, 8 and 9 are not anticipated under 35 U.S.C. §102(e) by Cockerill et al (U.S. 5,786,237).

While the Cockerill et al document does mention dividing into 1x4 or 1x3 or 1x2 or 1x1, it does not specifically state that it would make the division as a result of the testing as do applicant's claims, making 4 element divisions if possible, but if not, making 2 element or 1 element divisions. The cited document, in contrast, appears to be pre-set for cutting a specific size pattern, either 1x4, 1x3, 1x2 or 1x1. It does not teach that a decision is made based on testing of whether groups of 4 pieces are possible, and if not, then whether groups of 2 are possible, and if not, then into single pieces. Therefore, applicant's claimed invention is different, in that applicant, in accordance with the claims, is trying to maximize the number of higher yield components (4 piece components) but will make the

smaller 2 or 1 piece components when that is the only size available. Thus, applicant's invention will not waste smaller 2 or 1 element pieces from the wafer. The cited document, in contrast, if set to cut 1x4 pieces, will make a cutting pattern that will cut out only the preset 1x4 size pieces and if there are sections of the wafer that have 1x1 or 1x2 pieces only available, the cited document will leave those pieces wasted. Applicant's claimed invention will successfully employ those 1 and 2 piece groupings, leaving them unwasted.

Claim 5 includes the following steps:

- forming a plurality of identical semiconductor chips on a semiconductor wafer;

- carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer;

- dividing one of a plurality of pieces of said semiconductor chips on the basis of a result of said quality test;

- the plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to

be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible as a result of said quality test.

Nowhere does Cockerill et al discuss dividing into groups of 4, 2 or 1 depending on the results of a quality test. Cockerill et al merely divide the wafer to produce as many of a single array size (1x4 is the given example) that is currently desired to be produced. It does not teach or suggest dividing the wafer groups into the largest size (4, 2, or 1) that is possible given the results of testing. Cockerill mentions (column 3, lines 44-49) that "an optimizing algorithm may be used to determine the dicing pattern to optimize the total yield of (e.g. 1x4) arrays from the wafer." This does not teach applicant's system that will divide the wafer to produce as many of the group of 4 chips as possible, but will also divide the other portions of the wafer into groups of two, those portions having been determined by testing to not be suitable for grouping as 4 chips. Further, those portions of the wafer that do not support grouping as two, are divided into groups of one. In contrast, the Cockerill et al system will only divide into the set group size that is currently being produced, groups of 1 by 4 being the illustrated example in Cockerill. The Cockerill et al document does not mention nor

does it appreciate that it would be desirable to employ the results of testing to divide out all the chips on the wafer, even those that while functional (based on testing results), are such that grouping in the largest desired size (groups of 4) is not possible, but grouping in a smaller size group (groups of 2 or 1) is possible so that some useful chips will still be available even if not in the largest desired size.

Independent claim 8 is similar to claim 5, but has additional steps related to of carrying out wiring, resin sealing, terminal formation for a plurality of said semiconductor chips formed on said semiconductor wafer. For reasons corresponding to those presented above with respect to claim 5, claim 8 should also be allowable.

Dependent claims 6 and 9, depending on claims 5 and 8 respectively, should also be allowable as depending from allowable claims. Claims 6 and 9 add that the chips are memory chips.

By employing applicant's claimed method, full use of all the good chips on a wafer will be made, by dividing the wafer in to 2 chip size portions where 4 chip portions are not available because of testing results, and by dividing to 1 chip size portions if neither 4 chip nor 2 chip size portions not available.

In view of these points above, it is respectfully submitted that the rejection under 35 U.S.C. §102(e) should not be sustained.

CONCLUSION

In view of the foregoing, it is submitted that claims 5, 6, 8 and 9 of this application are patentable, and it is accordingly requested that the Examiner's final rejection be reversed and that allowance of this application be directed.

Respectfully submitted,

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APPENDIX OF CLAIMS

5. (previously amended) A method for manufacturing the semiconductor device, comprising:

a first step of forming a plurality of identical semiconductor chips on a semiconductor wafer;

a second step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer; and

a third step of dividing one of a plurality of pieces of said semiconductor chips on the basis of a result of said quality test,

wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are

determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible as a result of said quality test.

6. (original) The method for manufacturing the semiconductor device according to claim 5, wherein said semiconductor chips are memory chips.

8. (previously amended) A method for manufacturing the semiconductor device, comprising:

a first step of forming a plurality of identical semiconductor ships on a semiconductor wafer;

a second step of carrying out wiring, resin sealing, terminal formation for a plurality of said semiconductor chips formed on said semiconductor wafer;

a third stop of carrying out a quality test of each of a plurality of said semiconductor chips, which is formed on said semiconductor wafer, by using said terminal formed by said second step; and

a fourth step of dividing one or a plurality of said semiconductor chips on the basis of a result of said quality test,

wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible, after said quality test is carried out.

9. (original) The method for manufacturing the semiconductor device according to claim 8, wherein said semiconductor chips are memory chips.